IN THE CLAIMS

Please cancel Claim 13-15 and Amend the remaining Claims in accordance with the following mark-up copy:

1. (Currently Amended) An interface for interconnecting electronic components, comprising:

a first input for receiving a single-ended data signal;

a second input for receiving a non-inverted signal of a differential data signal pair;

a third input for receiving an inverted signal of said differential data signal pair; and

a receiver coupled to said first input, said second input and said third input for detecting a value of said single-ended data signal, said detected value representative of a binary logic state of said single-ended data signal, wherein detection of said value of said single-ended data signal is made in conformity with a common mode value of said differential data signal pair, and wherein said receiver comprises a first differential comparator coupled to said second input and said third input for detecting a binary logic state of said differential data signal pair.

2. (Currently Amended) The interface of Claim 1, wherein said receiver further comprises[[:]]

~~a differential comparator coupled to said second input and~~

~~said third input for detecting a binary logic state of said differential data signal pair; and~~

a singlential comparator coupled to said differential comparator and further coupled to said first input, said second input and said third input for detecting said value of said single-ended data signal in conformity with said common mode value of said differential data signal pair.

3. (Previously Amended) The interface of Claim 2, wherein said singlential comparator sums said non-inverted signal of said differential data signal pair and said inverted signal of said differential data signal pair to provide a reference value for detecting said single-ended data signal.

4. (Previously Amended) The interface of Claim 2, wherein said singlential comparator comprises means for summing said non-inverted signal of said differential data signal pair and said inverted signal of said differential data signal pair to provide a reference for detecting said value of said single-ended data signal.

5. (Previously Amended) The interface of Claim 3, wherein said singlential comparator comprises:

a first transistor having a gate coupled to said first input;

a second transistor having a gate coupled to said second input;

a third transistor having a gate coupled to said third input; and

a current source coupled to a channel connection of said first transistor, a channel connection of said second transistor and a channel connection of said third transistor, whereby said singlential comparator detects said value of said single-ended data signal in conformity with an average of a second value of said non-inverted signal and a third value of said inverted signal of said differential data signal pair.

6. (Currently Amended) The interface of Claim 5, wherein said first differential comparator comprises:

a fourth transistor having a gate coupled to said second input; and

a fifth transistor having a gate coupled to said third input and a first channel connection coupled to a resistor for providing active mode operation; and

a current source coupled to a channel connection of said fourth transistor and a second channel connection of said fifth transistor, whereby said differential comparator detects a difference between said value of said non-inverted signal and said value of said inverted signal of said differential data signal pair, and wherein a gain of said first differential

comparator in an active region of operation is equal to a gain of said singlential comparator.

7. (Currently Amended) The interface of Claim 2, wherein said receiver further comprises a multiplexer for producing a data output signal corresponding to said single-ended data signal, having a first input coupled to an output of said first differential comparator, a second input coupled to an inverted output of said first differential comparator, and a select input coupled to said output of said first differential comparator and an output of said singlential comparator such that said output of said first differential comparator is selected when said single-ended signal is at an equal logic value with said differential data signal pair and wherein said inverted output of said first differential comparator is selected when said single-ended signal and said differential data signal pair are at unequal logic levels.

8. (Currently Amended) The interface of Claim 7, wherein said receiver further comprises:

a first latch for coupling said first differential comparator to said multiplexer, said first latch having an input coupled to said output of said first differential comparator and an output coupled to said first input of said multiplexer;

an inverter having an input coupled to said output of said

first latch for producing said inverted output of said first differential comparator and having an output coupled to said multiplexer;

a second latch for latching said output of said singlential comparator; and

an exclusive-OR gate having a first input coupled to said output of said first latch and a second input coupled to an output of said second latch and an output coupled to a select input of said multiplexer for selecting said output of said first latch when said single-ended data signal is at an equal logic value with said binary logic state of said differential data signal pair and for selecting said output of said inverter when said single-ended signal and said differential data signal pair are at unequal logic levels.

9. (Currently Amended) The interface of Claim 1, wherein said receiver further comprises:

~~a first differential comparator coupled to said second input and said third input;~~

a second differential comparator coupled to said second input and said first input;

a third differential comparator coupled to said third input and said first input; and

means for selecting between an output of said second differential comparator and an output of said third differential

comparator to produce a data output corresponding to said binary logic state of said single-ended data signal.

10. (Currently Amended) The interface of Claim 1, wherein said receiver further comprises:

~~a first differential comparator coupled to said second input and said third input;~~

a second differential comparator coupled to said first input and said second second input;

a third differential comparator coupled to said first input and said third input; and

a logic circuit coupled to said first differential comparator, said second differential comparator and said third differential comparator for selecting between an output of said second differential comparator and said third differential comparator to produce a data output corresponding to said binary logic state of said single-ended data signal.

11. (Previously Amended) The interface of Claim 10, wherein said logic circuit comprises:

a multiplexer for producing said data output corresponding to said binary logic state of said single-ended data signal;

a first latch having an input coupled to an output of said first differential comparator;

a second latch having an input coupled to an output of said

second differential comparator and an output coupled to a first input of said multiplexer;

a third latch having an input coupled to an output of said third differential comparator and an output coupled to a second input of said multiplexer;

a first exclusive-OR gate having inputs coupled to said input of said first latch and said output of said first latch for detecting a difference between a present state and a prior state of said output of said first differential comparator;

a second exclusive-OR gate having inputs coupled to said input of said second latch and said output of said second latch for detecting a difference between a present binary logic state and a prior binary logic state of said output of said second differential comparator; and

a third exclusive-OR gate having inputs coupled to an output of said first exclusive-OR gate and an output of said second exclusive-OR gate, and having an output coupled to a select input of said multiplexer, for performing said selecting.

12. (Previously Amended) The interface of Claim 11, further comprising a fourth exclusive-OR gate having inputs coupled to said input of said third latch and said output of said third latch for detecting a difference between said present binary logic state and said prior binary logic state of said output of said third differential comparator, and wherein said fourth

exclusive-OR gate has an output coupled to an input of said third exclusive-OR gate.

Claims 13-17 have been canceled.

18. (Currently Amended) A method for signaling over an electronic interface, said method comprising:

transmitting a differential data signal pair;

transmitting a single-ended data signal;

receiving said differential data signal pair;

detecting a value of said received differential data signal pair, wherein said detected value is representative of a binary logic state of said received differential data signal pair; and

detecting a value of said single-ended data signal in conformity with a common-mode value of said received differential data signal pair, wherein said detected value is representative of a binary logic state of said single-ended data signal.

19. (Currently Amended) The method of Claim 18, wherein said detecting a value of said single-ended data signal comprises:

deriving a reference from said differential pair of data signals; and

detecting a difference between said value of said single-ended data signal and said derived reference.

20. (Previously Amended) The method of Claim 19, wherein said deriving comprises summing currents proportional to a second value of a non-inverting signal of said differential data signal pair and a third value of an inverting signal of said differential data signal pair, and wherein said detecting of said difference between said value of said single-ended data signal and said derived reference comprises balancing a current proportional to said value of said single ended data signal against said summed currents.

21. (Currently Amended) The method of Claim 18, wherein said detecting a value of said single-ended data signal comprises:

comparing a third value of a non-inverting signal of said differential pair to a second value of an inverting signal of said differential pair;

comparing said value of said single-ended data signal to said third value of said non-inverting signal of said differential data signal pair;

comparing said value of said single-ended data signal to said second value of said inverting signal of said differential data signal pair; and

selecting between a result of said comparing of said third value to said second value and said comparing of said value of said single-ended data signal to said second value, in conformity with a result of said first comparing and said second comparing.

22. (Original) The method of Claim 21, wherein said selecting is further performed in conformity with a result of said third comparing.

RECORD OF TELEPHONIC INTERVIEW

On September 29, 2004, an interview was conducted with Primary Examiner Kenneth Wells. Both Andoh, et al. (U.S. 5.936,466) and Alexander, et al. (U.S. 5,936,469) were discussed with respect to the rejection of the Claims in the above-referenced Office Action, although the rejection in the above-referenced Office Action is based solely upon Andoh.

An Amendment is entered above, and the Primary Examiner agreed that the addition of the differential comparator to Claim 1 and the addition of the detecting a value of the differential data signal pair to Claim 18 would distinguish the invention from Andoh, overcoming the rejections of the above-referenced Office Action.

With respect to Alexander, the Primary Examiner indicated that Figure 4 of Alexander might anticipate the claims as amended, as transistors 58 and 82 of that Figure might be interpreted as a differential comparator in addition to the Examiner's construction of a singlential comparator from transistors 52, 80 and 54. Applicants disagreed and further agreed to provide analysis and argument demonstrating that the circuit of Figure 4 of Andoh is not capable of performing the functions recited in Claims 1 and 18.